DS28EC20
20Kb 1-Wire EEPROM

www.maxim-ic.com

GENERAL DESCRIPTION

The DS28EC20 is a 20480-bit, 1-Wire® EEPROM organized as 80 memory pages of 256 bits each. An additional page is set aside for control functions. Data is written to a 32-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, blocks of eight memory pages can be write protected or put in EPROM-Emulation mode, where bits can only be changed from a 1 to a 0 state. The DS28EC20 communicates over the single-conductor 1-Wire bus. The communication follows the standard 1-Wire protocol. Each device has its own unalterable and unique 64-bit ROM registration number that is factory lasered into the chip. The registration number is used to address the device in a multidrop 1-Wire net environment.

APPLICATIONS

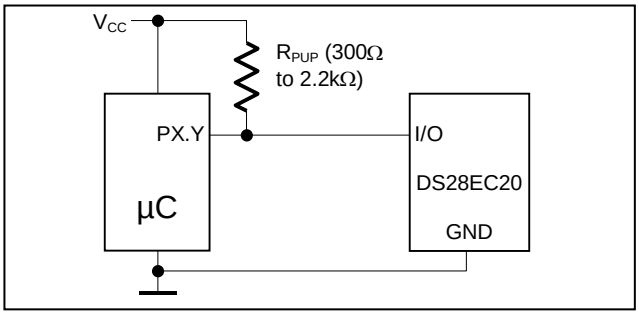
Device Authentication
IEEE 1451.4 Sensor TEDS
Ink/Toner Cartridges
Medical Sensors
PCB Identification
Wireless Base Stations

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS28EC20+	-40°C to +85°C	3 TO-92
DS28EC20+T	-40°C to +85°C	3 TO-92, T&R
DS28EC20P+	-40°C to +85°C	6 TSOC
DS28EC20P+T	-40°C to +85°C	6 TSOC, T&R

+ Denotes a lead-free package.
T = tape and reel

TYPICAL OPERATING CIRCUIT



Commands, bytes, and modes are capitalized for clarity.

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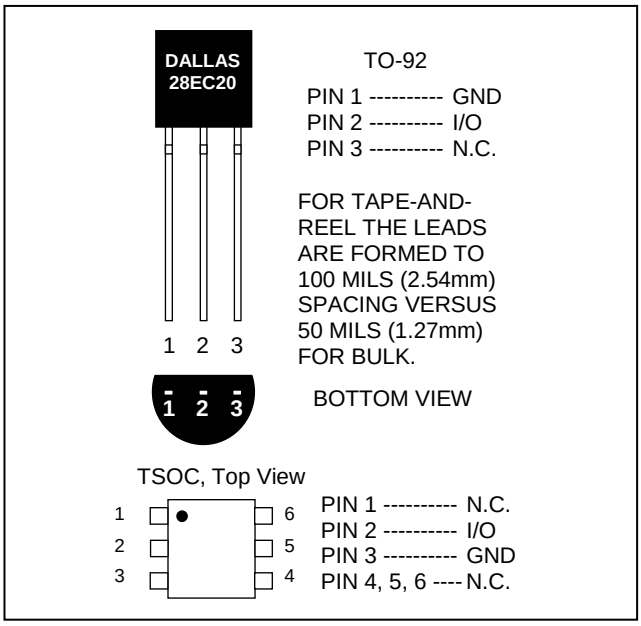
FEATURES

- 20480 Bits of Nonvolatile (NV) EEPROM Partitioned into Eighty 256-Bit Pages
- Individual 8-Page Groups of Memory Pages (Blocks) can be Permanently Write Protected or Put in OTP EPROM-Emulation Mode ("Write to 0")
- Read and Write Access Highly Backward-Compatible to Legacy Devices (e.g., DS2433)
- 256-Bit Scratchpad with Strict Read/Write Protocols Ensures Integrity of Data Transfer
- 200k Write/Erase Cycle Endurance at +25°C
- Unique Factory-Programmed 64-Bit Registration Number Ensures Error-Free Device Selection and Absolute Part Identity
- Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise
- Communicates to Host at 15.4kbps or 125kbps Using 1-Wire Protocol
- Low-Cost TO-92 Package
- Operating Range: 5V ±5%, -40°C to +85°C
- IEC 1000-4-2 Level 4 ESD Protection (8kV Contact, 15kV Air, Typical) for I/O Pin

PIN CONFIGURATION



REV: 091707

ABSOLUTE MAXIMUM RATINGS

I/O Voltage to GND	-0.5V, +6V
I/O Sink Current	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C, see Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O PIN GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 2)	4.75		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 4, 5)			1000	pF
Input Load Current	I_L	I/O pin at V_{PUP}	0.05	6.7	55	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	1.6		V_{PUP} - 1.8	V
Input Low Voltage	V_{IL}	(Notes 2, 8)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 6, 9)	2.5		V_{PUP} - 1.1	V
Switching Hysteresis	V_{HY}	(Notes 5, 6, 10)	0.30		1.30	V
Output Low Voltage	V_{OL}	At 4mA (Note 11)			0.20	V
Recovery Time (Notes 2, 12)	t_{REC}	Standard speed	5			µs
		Overdrive speed	2			
		Overdrive speed, directly prior to reset pulse	5			
Rising-Edge Hold-off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Timeslot Duration (Notes 2, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
I/O PIN, 1-Wire RESET, PRESENCE DETECT CYCLE						
Reset-Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence-Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence-Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 2, 15)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	
I/O PIN, 1-Wire WRITE						
Write-0 Low Time (Notes 2, 16, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	6		15.5	
Write-1 Low Time (Notes 2, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
I/O PIN, 1-Wire READ						
Read-Low Time (Notes 2, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read-Sample Time (Notes 2, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM						
Programming Current	I_{PROG}	(Note 19)			0.8	mA
Programming Time	t_{PROG}	(Note 20)			10	ms
Write/Erase Cycles (Endurance) (Notes 21, 22)	N_{CY}	At +25°C	200k			—
		At +85°C (worst case)	50k			
Data Retention (Notes 23, 24, 25)	t_{DR}	At +85°C (worst case)	40			years

Note 1: Specifications at T_A = -40°C are guaranteed by design only and not production-tested.
Note 2: System requirement.
Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system, 1-Wire recovery times, and current requirements during EEPROM programming. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required.
Note 4: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied the parasite capacitance does not affect normal communications.
Note 5: Guaranteed by design, characterization and/or simulation only. Not production tested.
Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage which is itself a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on I/O. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 7: Voltage below which, during a falling edge on I/O, a logic 0 is detected.
Note 8: The voltage on I/O needs to be less or equal to V_{ILMAX} at all times the master is driving I/O to a logic 0 level.
Note 9: Voltage above which, during a rising edge on I/O, a logic 1 is detected.
Note 10: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O has to drop by at least V_{HY} to be detected as logic 0.
Note 11: The I-V characteristic is approximately linear for voltages less than 1V.
Note 12: Applies to a single device attached to a 1-Wire line.
Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.
Note 14: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 15: Interval after t_{RSTL} during which a bus master is guaranteed to sample a logic 0 on I/O if there is a DS28EC20 present. Minimum limit is t_{PDHMAX}; maximum limit is $t_{PDHMIN} + t_{PDLMIN}$.
Note 16: Highlighted numbers are NOT in compliance with legacy 1-Wire product standards. See comparison table below.
Note 17: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.
Note 18: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.
Note 19: Current drawn from I/O during the EEPROM programming interval. During a programming cycle the voltage at I/O drops by $I_{PROG} \times R_{PUP}$ below V_{PUP}. If V_{PUP} and R_{PUP} are within their EC table limits, the residual I/O voltage meets the guaranteed-by-design minimum voltage requirements for programming.
Note 20: The t_{PROG} interval begins t_{REHMAX} after the trailing rising edge on I/O for the last time slot of the E/S byte for a valid copy scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.
Note 21: Write-cycle endurance is degraded as T_A increases.
Note 22: Not 100% production-tested; guaranteed by reliability monitor sampling.
Note 23: Data retention is degraded as T_A increases.
Note 24: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.
Note 25: EEPROM writes may become nonfunctional after the data retention time is exceeded. Long-time storage at elevated temperatures is not recommended; the device may lose its write capability after 10 years at +125°C or 40 years at +85°C.

PARAMETER	LEGACY VALUES				DS28EC20 VALUES			
	STANDARD SPEED		OVERDRIVE SPEED		STANDARD SPEED		OVERDRIVE SPEED	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (incl. t_{REC})	61µs	(undefined)	7µs	(undefined)	65µs*	(undefined)	8µs*	(undefined)
t_{RSTL}	480µs	(undefined)	48µs	80µs	480µs	640µs	48µs	80µs
t_{PDH}	15µs	60µs	2µs	6µs	15µs	60µs	2µs	6µs
t_{PDL}	60µs	240µs	8µs	24µs	60µs	240µs	8µs	24µs
t_{W0L}	60µs	120µs	6µs	16µs	60µs	120µs	6µs	15.5µs

* Intentional change, longer recovery time requirement due to modified 1-Wire front-end.

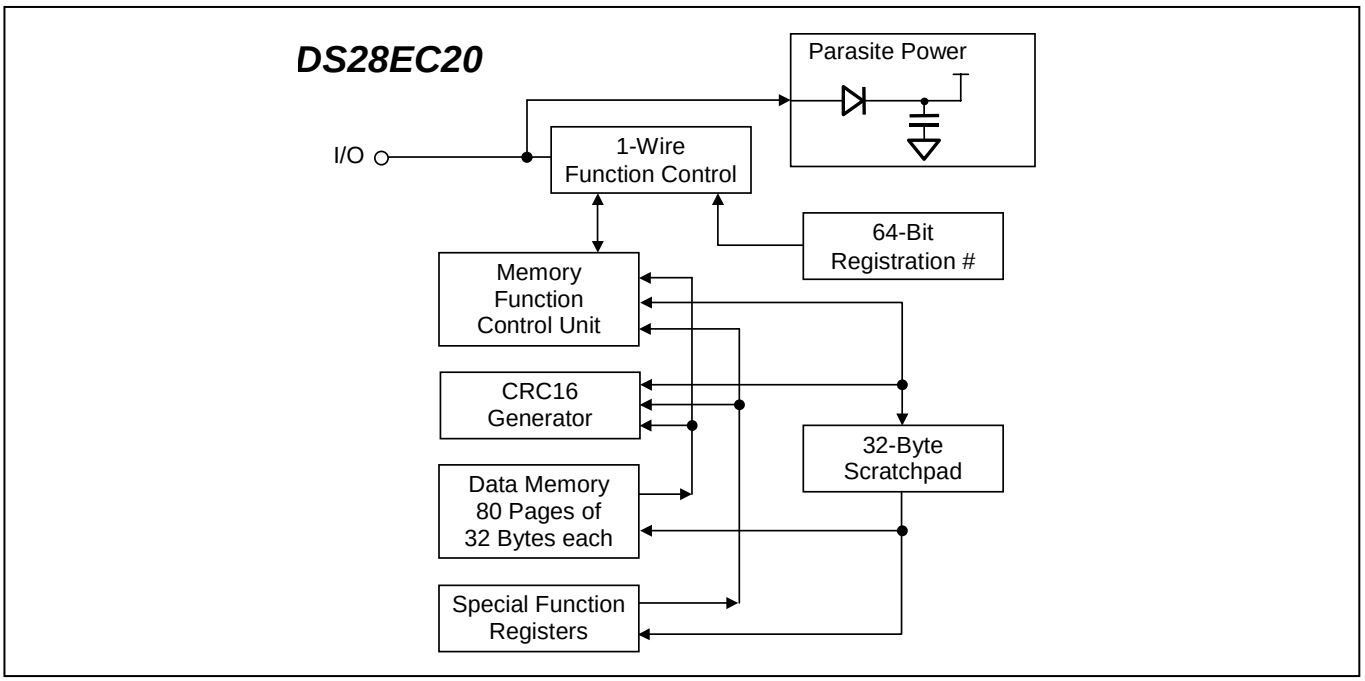
PIN DESCRIPTION

NAME	FUNCTION
I/O	1-Wire Bus Interface. Open drain, requires external pullup resistor.
GND	Ground Reference
N.C.	Not Connected

DESCRIPTION

The DS28EC20 combines 20Kb of data EEPROM with a fully featured 1-Wire interface in a single chip. The memory is organized as 80 pages of 256 bits each. In addition, the device has one page for control functions such as permanent write protection and EPROM-Emulation mode for individual 2048-bit (8-page) memory blocks. A volatile 256-bit memory page called the scratchpad acts as a buffer when writing data to the EEPROM to ensure data integrity. Data is first written to the scratchpad, from which it can be read back for verification before transferring it to the EEPROM. The operation of the DS28EC20 is controlled over the single-conductor 1-Wire bus. Device communication follows the standard 1-Wire protocol. The energy required to read and write the DS28EC20 is derived entirely from the 1-Wire communication line. Each DS28EC20 has its own unalterable and unique 64-bit registration number. The registration number guarantees unique identification and is used to address the device in a multidrop 1-Wire net environment. Multiple DS28EC20 devices can reside on a common 1-Wire bus and be operated independently of each other. Applications of the DS28EC20 include device authentication, analog-sensor calibration such as IEEE-P1451.4 Smart Sensors TEDS, ink and toner print cartridge identification, medical-sensor calibration data storage, PC board identification, and data for self-configuration of central office switches, wireless base stations, PBXs, or other modular-based rack systems. The DS28EC20 provides a high degree of backward compatibility with the DS2433. Besides the different family codes, the only protocol change that is required on an existing DS2433 implementation is a lengthening of the programming duration (t_{PROG}) from 5ms to 10ms.

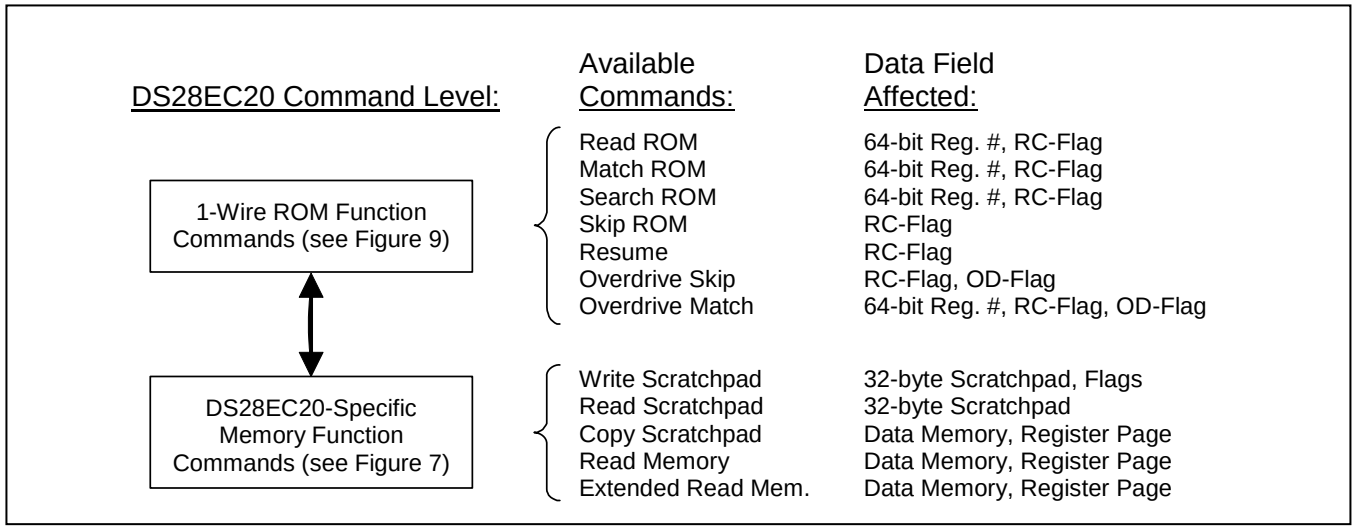
Figure 1. Block Diagram



OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28EC20. The DS28EC20 has four main data components: 1) 64-bit registration number, 2) 32-byte scratchpad, 3) eighty 32-byte pages of EEPROM, and 4) special function registers. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM (network) function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Resume, 6) Overdrive Skip ROM, or 7) Overdrive Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the five memory function commands. The protocol for these commands is described in Figure 7. All data is read and written least significant bit first.

Figure 2. Hierarchical Structure for 1-Wire Protocol



64-BIT LASERED ROM

Each DS28EC20 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in *Application Note 27*: *Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor iButton® Products* (www.maxim-ic.com/AN27).

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

Figure 3. 64-Bit Lasered ROM

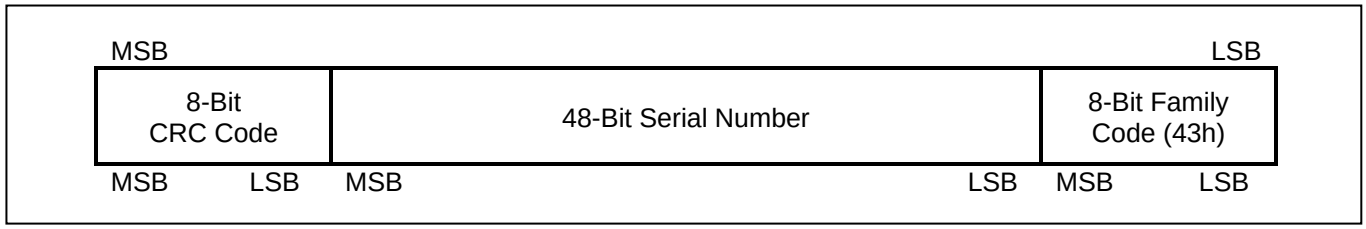


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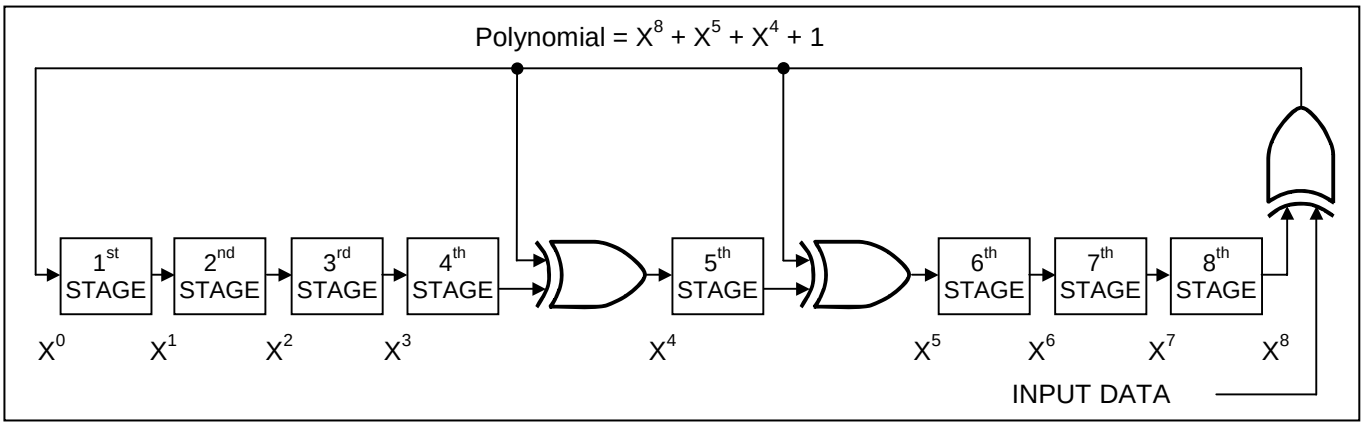
Figure 4. 1-Wire CRC Generator



MEMORY

Data memory and special function registers are located in a linear address space, as shown in Figure 5. The data memory and the registers have unrestricted read access. The data memory consists of 80 pages of 32 bytes each. Eight adjacent pages form one 2Kb block. Each block can be individually set to open (default), write protected, or EPROM mode by setting the associated protection byte in the register page, which starts at address 0A00h. Besides the 10 block protection control bytes (one for each 2Kb data memory block) the register page contains 20 bytes of user EEPROM plus a memory block lock byte and a register page lock byte. Starting at address 0A20h, the DS28EC20 has a read-only memory page that stores a factory byte and a 2-byte field reserved for a factory-administered service to program manufacturer identification. All other bytes of that page are reserved. The manufacturer ID can be a customer-supplied identification code that assists the application software in identifying the product the DS28EC20 is associated with. Contact the factory to set up and register a custom manufacturer ID. In addition to the EEPROM, the device has a 32-byte volatile scratchpad. Writes to the EEPROM array are a two-step process. First, data is written to the scratchpad, and then copied into the main array. The user can verify the data in the scratchpad prior to copying.

The protection control registers, along with the Memory Block Lock byte, determine whether write protection, EPROM mode, or copy protection is enabled for each of the 10 data memory blocks. A value of 55h sets write protection for the associated memory block. A value of AAh sets EPROM mode. The Memory Block Lock byte, if programmed to either 55h or AAh, sets copy protection for all write-protected data memory blocks. Blocks in EPROM mode are not affected. Programming the Register Page Lock byte to either 55h or AAh copy protects the entire register page. The protection control registers and the Lock bytes write protect themselves if set to 55h or AAh. Any other setting leaves them open for unrestricted write access. See the *Copy Protection* section for explanation of copy protect vs. write protect.

Write Protection: Write protection prevents data from being changed, but does not block the copy-scratchpad function; this allows the memory to be reprogrammed with the same data. In EEPROM devices digital information is stored as electrical charge (electrons) on floating gates. Quantum mechanical effects allow electrons to be transported in large numbers to and from the floating gate for programming and erasing memory cells. Electrons leave the floating gate at a temperature-dependent rate. The higher the temperature, the faster is the rate at which electrons escape. This rate is expressed as *Data Retention* in the EC table. Reprogramming the memory returns the charge to the original value for a full data retention time. This is particularly useful in applications where data retention is a concern, e.g., at high temperatures.

Copy Protection: Copy protection blocks the execution of the copy-scratchpad function. This feature achieves a higher level of security, and should only be used after all write-protected locations and their associated protection control bytes are set to their final values. Copy protection does not prevent copying data from one device to another.

Figure 5. Memory Map

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES (NOTES)
0000h to 00FFh	R/(W)	Data Memory Pages 0 to 7 (Block 0)	(Protection controlled by address 0A00h)
0100h to 01FFh	R/(W)	Data Memory Pages 8 to 15 (Block 1)	(Protection controlled by address 0A01h)
0200h to 02FFh	R/(W)	Data Memory Pages 16 to 23 (Block 2)	(Protection controlled by address 0A02h)
0300h to 03FFh	R/(W)	Data Memory Pages 24 to 31 (Block 3)	(Protection controlled by address 0A03h)
0400h to 04FFh	R/(W)	Data Memory Pages 32 to 39 (Block 4)	(Protection controlled by address 0A04h)
0500h to 05FFh	R/(W)	Data Memory Pages 40 to 47 (Block 5)	(Protection controlled by address 0A05h)
0600h to 06FFh	R/(W)	Data Memory Pages 48 to 55 (Block 6)	(Protection controlled by address 0A06h)
0700h to 07FFh	R/(W)	Data Memory Pages 56 to 63 (Block 7)	(Protection controlled by address 0A07h)
0800h to 08FFh	R/(W)	Data Memory Pages 64 to 71 (Block 8)	(Protection controlled by address 0A08h)
0900h to 09FFh	R/(W)	Data Memory Pages 72 to 79 (Block 9)	(Protection controlled by address 0A09h)
0A00h* to 0A09h*	R/(W)	Protection Control Blocks 0 to 9	55h: Write protected; AAh: EPROM mode. Address 0A00h is associated with Block 0, address 0A01h with Block 1, etc.
0A0Ah to 0A1Dh	R/(W)	User EEPROM	(Protection controlled by address 0A1Fh)
0A1Eh*	R/(W)	Memory Block Lock	(See text)
0A1Fh*	R/(W)	Register Page Lock	(See text)
0A20h	R	Factory Byte	(55h ➔ no valid manufacturer ID, AAh ➔ 0A23h to 0A24h are a valid Manufacturer ID)
0A21h to 0A22h	R	Factory Trim Bytes	(Unspecified value)
0A23h to 0A24h	R	Manufacturer ID	Validity depends on factory byte
0A25h to 0A3Fh	R	Reserved	(Unspecified value)

** Once programmed to AAh or 55h this address becomes read-only. All other codes can be stored but neither write-protect the address nor activate any function.*

ADDRESS REGISTERS AND TRANSFER STATUS

The DS28EC20 employs three address registers: TA1, TA2, and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is read. Register E/S is a read-only transfer status register used to verify data integrity with write commands. ES bits E[4:0] are loaded with the incoming T[4:0] on a Write Scratchpad command and increment on each subsequent data byte. This is, in effect, a byte-ending offset counter within the 32-byte scratchpad. Bit 5 of the E/S register, called PF, is set if the number of data bits sent by the master is not an integer multiple of 8 or if the data in the scratchpad is not valid due to a loss of power. A valid write to the scratchpad clears the PF bit. Bit 6 has no function; it always reads 0. The highest valued bit of the E/S register, called authorization accepted (AA), is valid only if the PF flag reads 0. If PF is 0 and AA is 1, the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

Figure 6. Address Registers

Bit #	7	6	5	4	3	2	1	0
Target Address (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
Target Address (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
Ending Address with Data Status (E/S) (Read Only)	AA	0	PF	E4	E3	E2	E1	E0

WRITING WITH VERIFICATION

To write data to the DS28EC20, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Under certain conditions (see the *Write Scratchpad Command* section) the master receives an inverted CRC16 of the command, address (actual address sent), and data at the end of the Write Scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated itself to decide if the communication was successful and precede to the Copy Scratchpad command. If the master could not receive the CRC16, it should send the Read Scratchpad command to verify data integrity. As a preamble to the scratchpad data, the DS28EC20 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad or there was a loss of power since data was last written to the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the device did not recognize the Write command. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue reading and verifying every data byte. After the master has verified the data, it can send the Copy Scratchpad command, for example. This command must be followed exactly by the data of the three address registers TA1, TA2, and E/S. The master should obtain the contents of these registers by reading the scratchpad. As soon as the DS28EC20 has received these bytes correctly, it starts copying the scratchpad data to the requested location, provided that the target memory is not copy protected, the PF flag is cleared, and there was no Read Memory or Extended Read Memory command issued between Write Scratchpad and Copy Scratchpad.

MEMORY FUNCTION COMMANDS

The *Memory Function Flow Chart* (Figure 7) describes the protocols necessary for accessing the memory of the DS28EC20. The target address registers TA1 and TA2 are used for both read and write. To prevent accidental changes to the data memory or control registers the device employs a BS-flag indicating a “bad sequence”. The communication between master and DS28EC20 takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the Overdrive mode, the DS28EC20 assumes standard speed.

WRITE SCRATCHPAD COMMAND [0Fh]

The Write Scratchpad command applies to the data memory and the writable addresses in the register page. After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset of T[4:0]. The ES bits E[4:0] are loaded with the starting byte offset, and increment with each subsequent byte. Effectively, E[4:0] is the byte offset of the last full byte written to the scratchpad. Only full bytes are accepted. If the last byte is incomplete its content is ignored and the partial byte flag PF is set. The PF flag is also set if the master ends the command before a complete target address is transmitted. The PF and BS flags are both cleared when a complete target address is received.

When executing the Write Scratchpad command, the CRC generator inside the DS28EC20 (Figure 13) calculates a 16-bit CRC of the entire data stream, starting at the command code and ending at the last data byte as sent by the master. This CRC is generated using the CRC16 polynomial ($X^{16} + X^{15} + X^2 + 1$) by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses TA1 and TA2 as supplied by the master, and all the data bytes. The master can end the Write Scratchpad command at any time. However, if the end of the scratchpad is reached (E[4:0] = 11111b), the master can send 16 read-time slots to receive the CRC generated by the DS28EC20.

If a Write Scratchpad is attempted to a write-protected location, the scratchpad is loaded with the data already in memory, rather than the data transmitted. Similarly, if the target address page is in EPROM mode, the scratchpad is loaded with the bitwise logical AND of the transmitted data and the data already in memory.

The DS28EC20’s memory address range is 0000h to 0A3Fh. If the bus master sends a target address higher than this, the DS28EC20’s internal circuitry sets the four most significant address bits to zero as they are shifted into the internal address register. The Read Scratchpad command reveals the modified target address. The master identifies such address modifications by comparing the target address read back to the target address transmitted. If the master does not read the scratchpad, a subsequent Copy Scratchpad command does not work since the most significant bits of the target address the master sends do not match the value the DS28EC20 expects.

READ SCRATCHPAD COMMAND [AAh]

The Read Scratchpad command allows verifying the target address and the integrity of the scratchpad data. After issuing the command code, the master begins reading. The first two bytes are the target address. The next byte is the Ending Offset/Data Status byte (E/S) followed by the scratchpad data beginning at the byte offset (T[4:0]). The scratchpad data can be different from what the master originally sent. This is of particular importance if the target address is within the register page or a page in either Write Protection or EPROM modes. See the *Write Scratchpad Command* section for details. The master should read through the end of the scratchpad, after which it receives an inverted CRC16, based on data as it was sent by the DS28EC20. If the master continues reading after the CRC, all data are logic 1s.

Figure 7-1. Memory Function Flow Chart

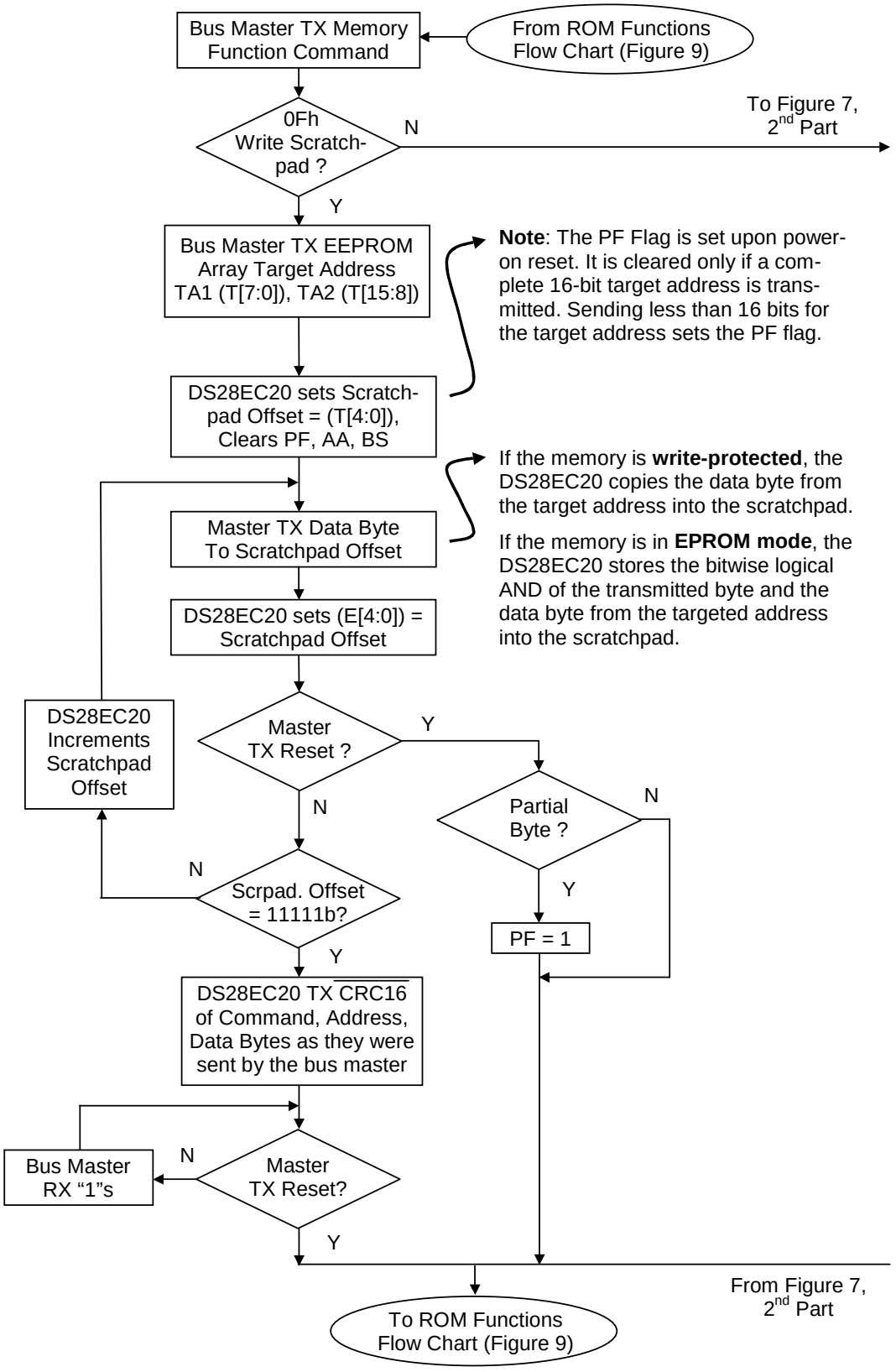


Figure 7-2. Memory Function Flow Chart (continued)

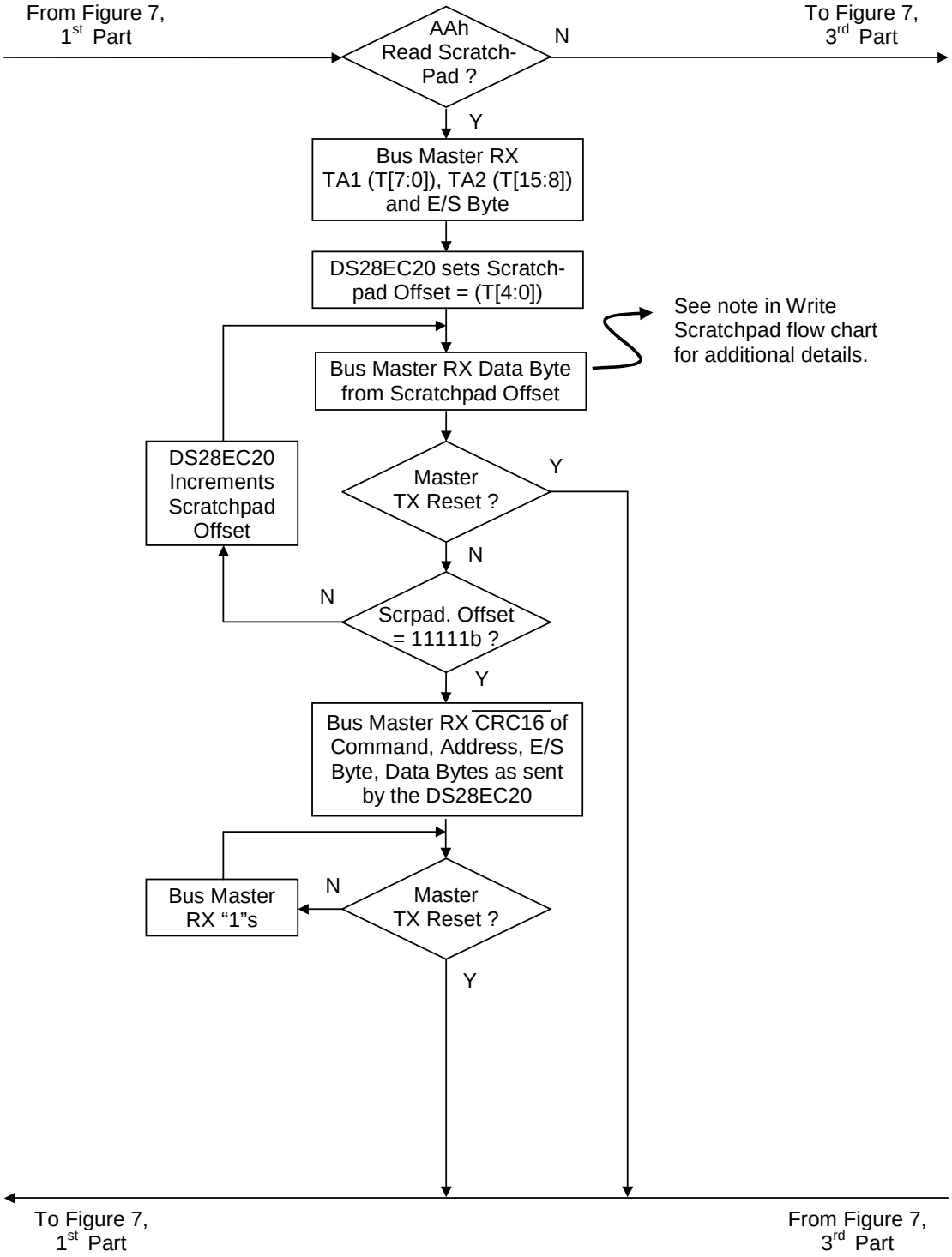


Figure 7-3. Memory Function Flow Chart (continued)

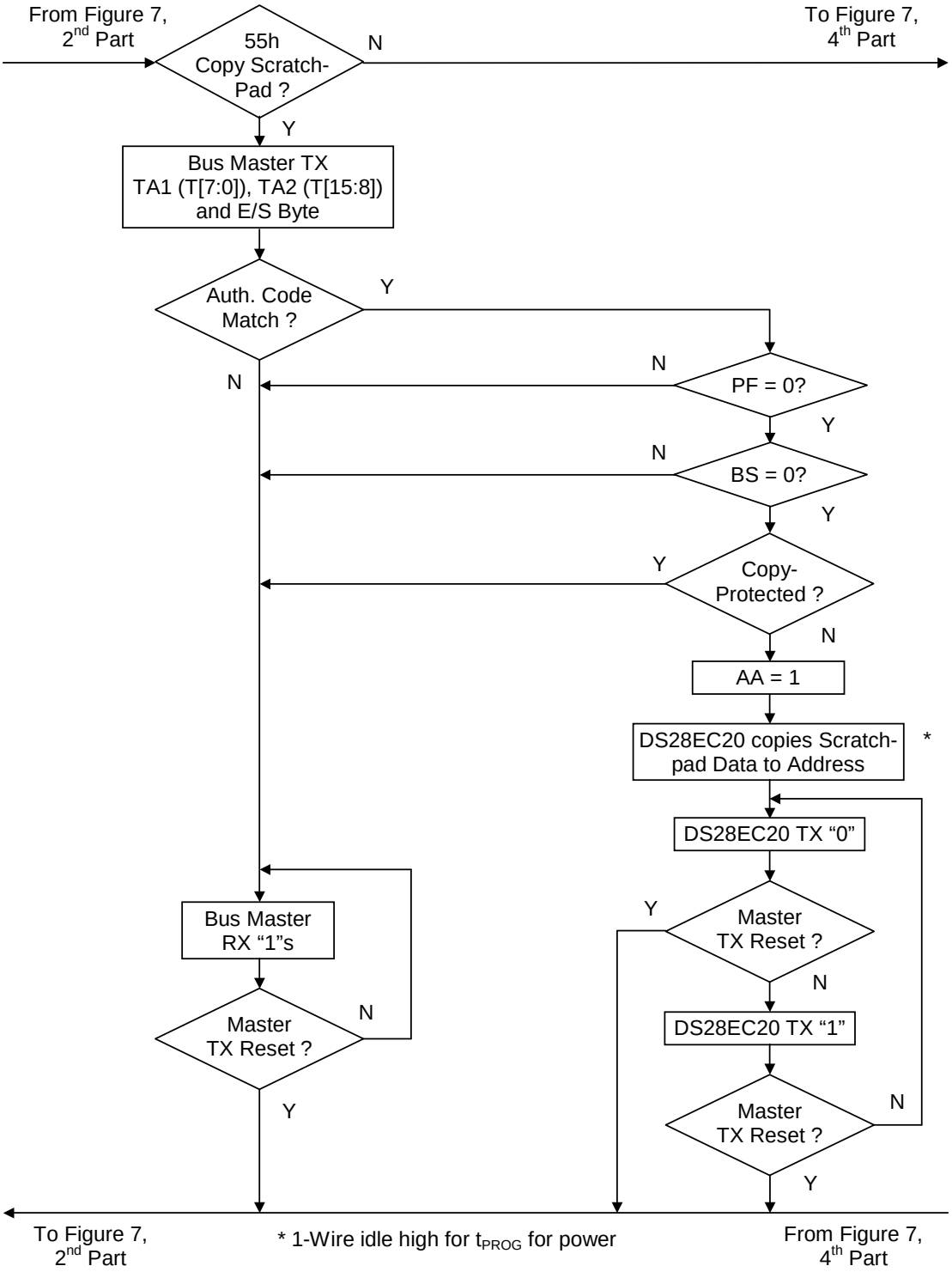
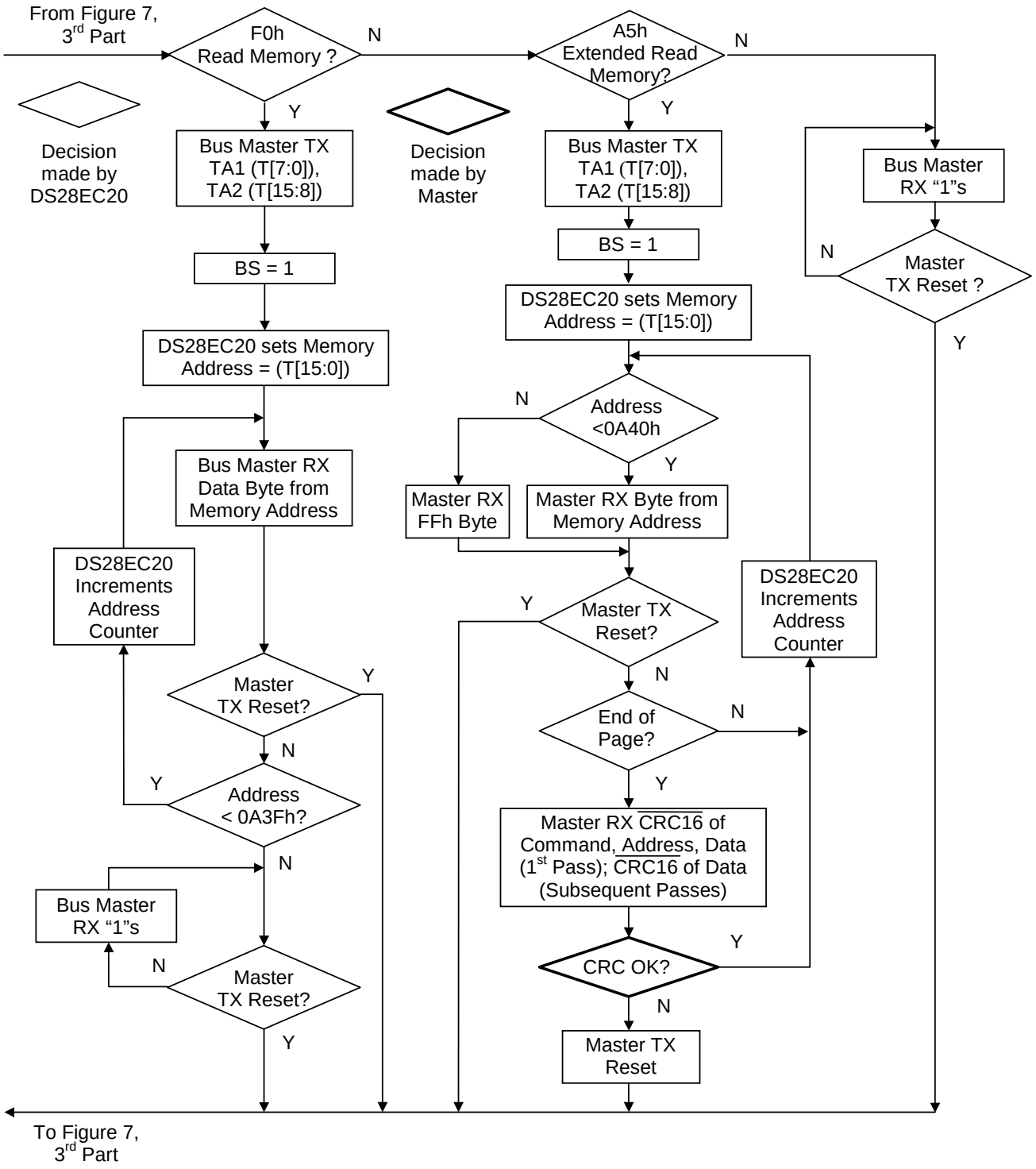


Figure 7-4. Memory Function Flow Chart (continued)



COPY SCRATCHPAD [55h]

The Copy Scratchpad command is used to copy data from the scratchpad to the data memory and the writable sections of the register page. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which should have been obtained by an immediately preceding Read Scratchpad command. This 3-byte pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the target address is valid, the PF and BS flag are not set, and the target memory is not copy protected, the AA flag is set and the copy begins. The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset is copied to memory, starting at the target address. Anywhere from 1 to 32 bytes can be copied with this command. The duration of the device's internal data transfer is t_{PROG} during which the 1-Wire bus must be idle or actively pulled high. Active pullup is optional for this device. A pattern of alternating 0s and 1s are transmitted after the data has been copied until the master issues a reset pulse. If the PF flag or BS flag is set or the target memory is copy protected, the copy does not begin and the AA flag is not set. The BS flag ensures that Copy Scratchpad is not executed (blocked) if there was a Read Memory or Extended Read Memory between Write Scratchpad and Copy Scratchpad.

READ MEMORY [F0h]

The Read Memory command is the general function to read from the DS28EC20. After issuing the command, the master must provide a 2-byte target address, which should be in the range of 0000h to 0A3Fh. If the target address is higher than 0A3Fh, the DS28EC20 changes the upper four address bits to 0. After the address is transmitted, the master reads data starting at the (modified) target address and can continue until address 0A3Fh. If the master continues reading, the result is FFh. The Read Memory command sequence can be ended at any point by issuing a reset pulse. Note that the target address provided with the Read Memory flow overwrites the target address that was specified with a previously issued Write Scratchpad command. Since the command also sets the BS flag, a subsequent Copy Scratchpad command fails even if the authorization pattern matches.

EXTENDED READ MEMORY [A5h]

This command works essentially the same way as Read Memory, except for the 16-bit CRC that the DS28EC20 generates and transmits following the last data byte of a memory page. The CRC generated by this command uses the same polynomial as the Write Scratchpad command. After issuing the command, the master must provide a 2-byte target address, which should be in the range of 0000h to 0A3Fh. If the target address is higher than 0A3Fh, the DS28EC20 changes the upper four address bits to 0. After the address is transmitted, the master reads data starting at the (modified) target address and continuing until the end of a 32-byte page is reached. At that point the bus master receives an inverted 16-bit CRC. If the master continues reading it receives data starting at the beginning of the next page, followed again by the inverted CRC for that page. Reading beyond the end of the memory is permissible, but the result is FFh. The Extended Read Memory command sequence can be ended at any point by issuing a reset pulse. Note that the target address provided with the Extended Read Memory flow overwrites the target address that was specified with a previously issued Write Scratchpad command. Since the command also sets the BS flag, a subsequent Copy Scratchpad command fails even if the authorization pattern matches.

1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS28EC20 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

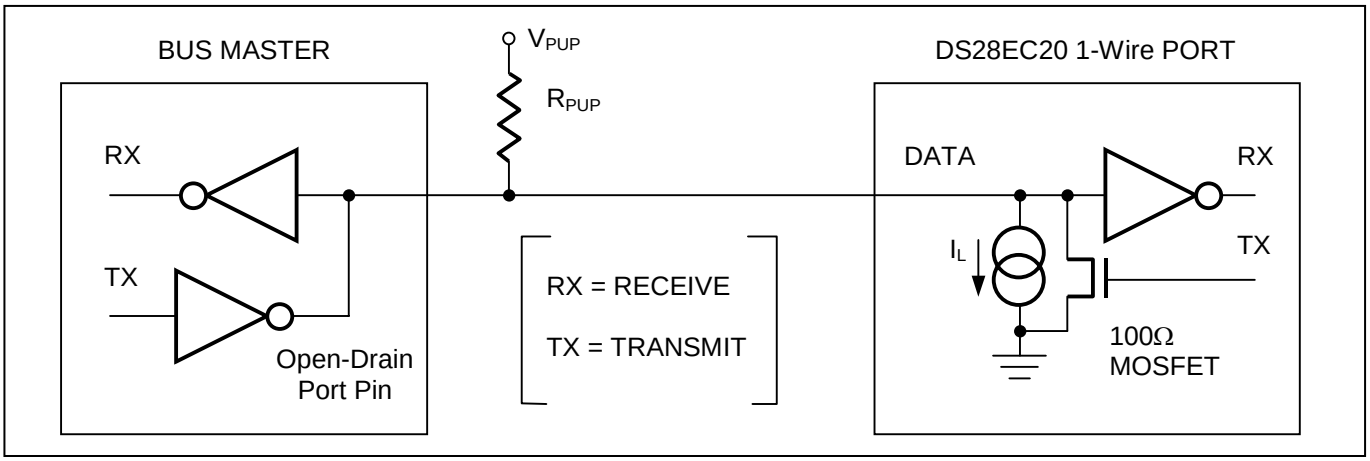
HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or tri-state outputs. The 1-Wire port of the DS28EC20 is open drain with an internal circuit equivalent to that shown in Figure 8.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28EC20 supports both a standard and overdrive communication speed of 15.4kbps (max) and 125kbps (max), respectively. Note that legacy 1-Wire products support a standard communication speed of 16.3kbps and overdrive of 142kbps. The slightly reduced rates for the DS28EC20 are a result of additional recovery times, which in turn were driven by a 1-Wire physical interface enhancement to improve noise immunity. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28EC20 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus can be reset.

Figure 8. Hardware Configuration



TRANSACTION SEQUENCE

The protocol for accessing the DS28EC20 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28EC20 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28EC20 supports. All ROM function commands are 8 bits long. See Figure 9 for list of these commands.

READ ROM [33h]

This command allows the bus master to read the DS28EC20's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

MATCH ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28EC20 on a multidrop bus. Only the DS28EC20 that exactly matches the 64-bit ROM sequence responds to the following memory function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the bus's wired-AND property, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* (www.maxim-ic.com/AN187) for a detailed discussion, including an example.

SKIP ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a Read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

RESUME [A5h]

To maximize the data throughput in a multidrop environment, the Resume function is available. This function checks the status of the RC bit and, if it is set, directly transfers control to the memory functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command function.

OVERDRIVE SKIP ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS28EC20 in the Overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into Overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

OVERDRIVE MATCH ROM [69h]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS28EC20 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS28EC20 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or successful Overdrive Match command remain in Overdrive mode. All overdrive-capable slaves return to standard speed at the next Reset Pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

Figure 9-1. ROM Functions Flow Chart

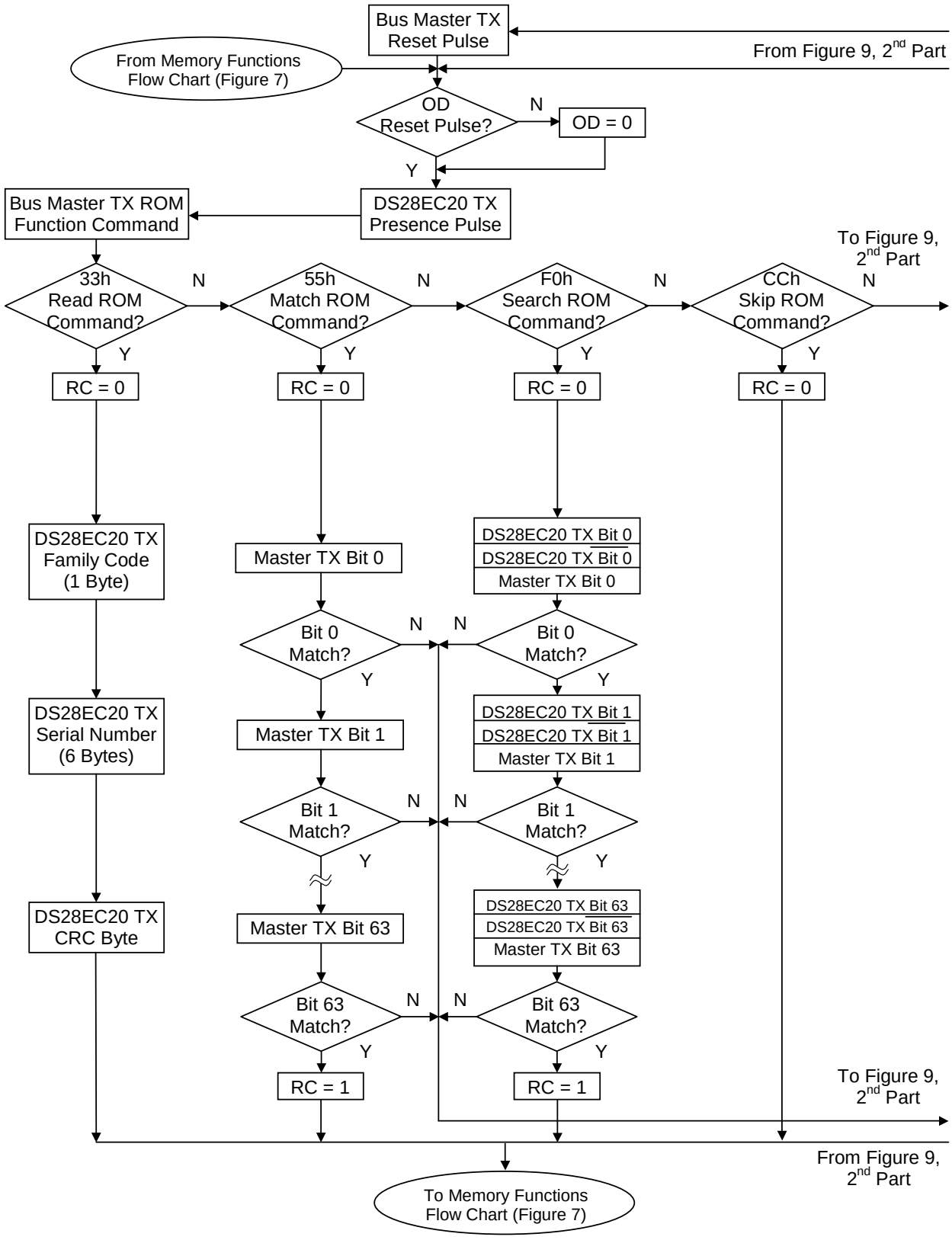
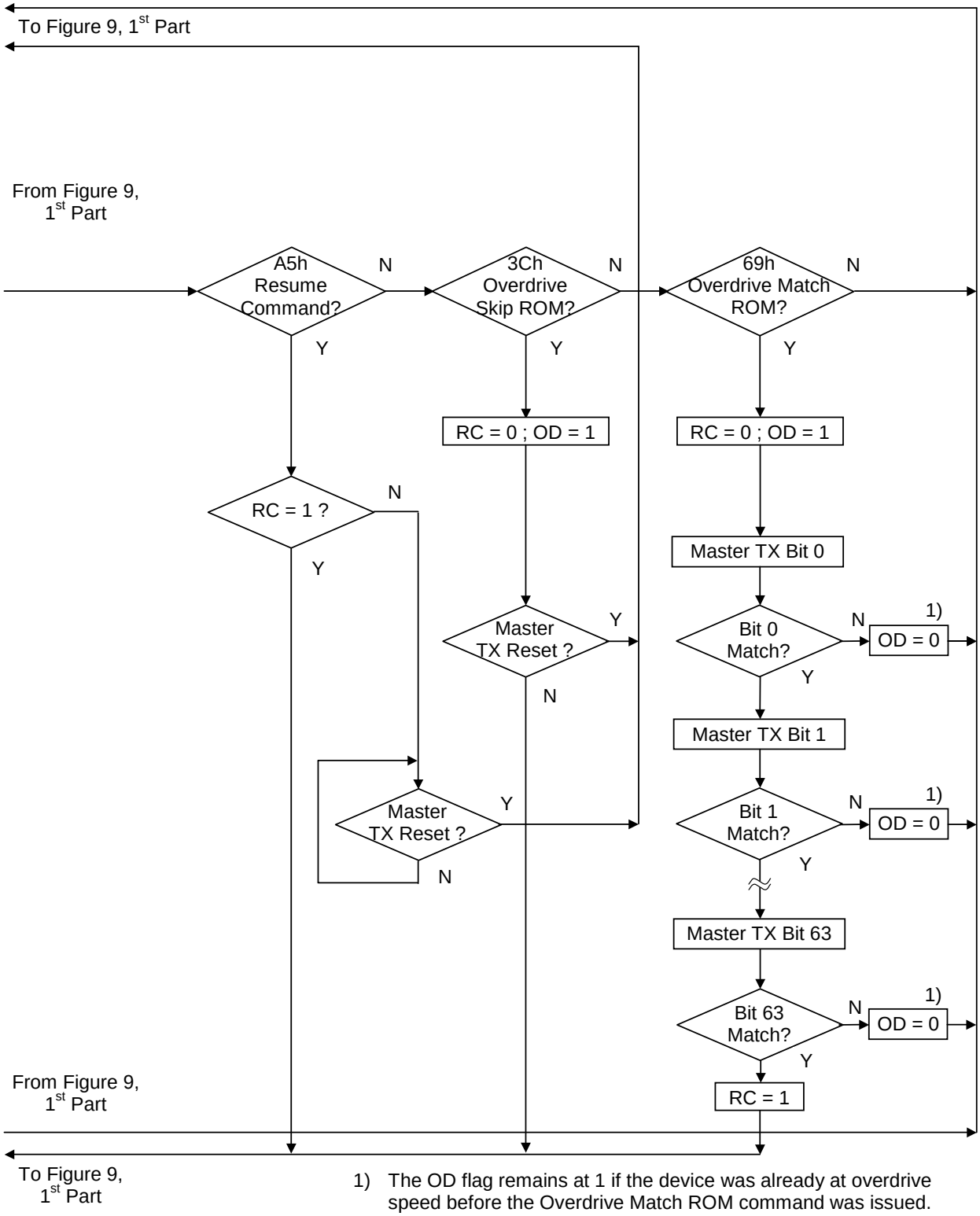


Figure 9-2. ROM Functions Flow Chart (continued)



1) The OD flag remains at 1 if the device was already at overdrive speed before the Overdrive Match ROM command was issued.

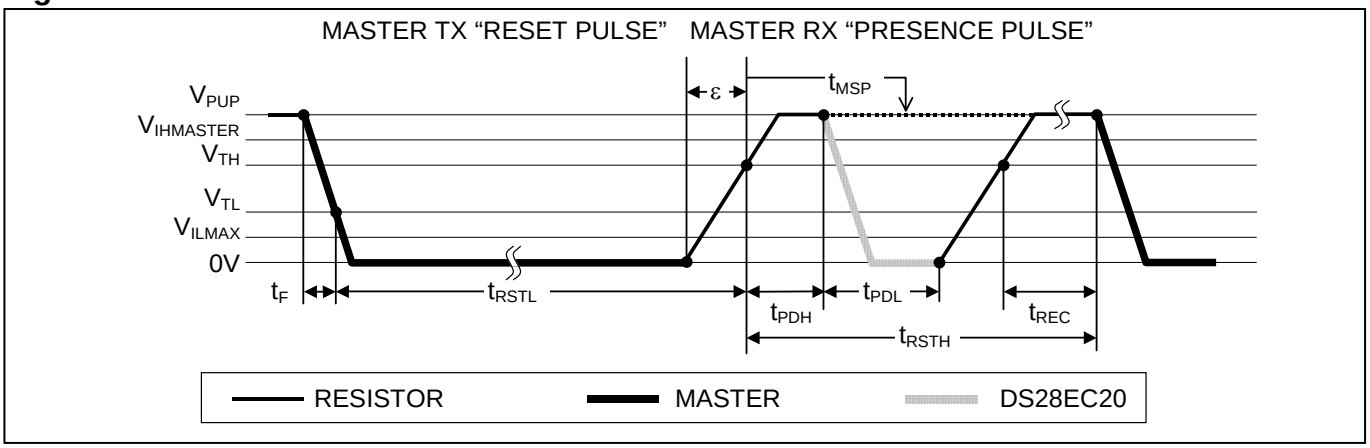
1-Wire SIGNALING

The DS28EC20 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28EC20 can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the Overdrive mode, the DS28EC20 communicates at standard speed. While in Overdrive mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 10 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28EC20 when determining a logical level, not triggering any events.

Figure 10 shows the initialization sequence required to begin any communication with the DS28EC20. A reset pulse followed by a presence pulse indicates that the DS28EC20 is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for t_{RSTL} + t_F to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the Overdrive mode, returning the device to standard speed. If the DS28EC20 is in Overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive mode. If the device is in Overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined.

Figure 10. Initialization Procedure: Reset and Presence Pulse



After the bus master has released the line it goes into Receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor, or in case of a DS2482-x00 or DS2480B driver, by active circuitry. When the threshold V_{TH} is crossed, the DS28EC20 waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS28EC20 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read-/Write-Time Slots

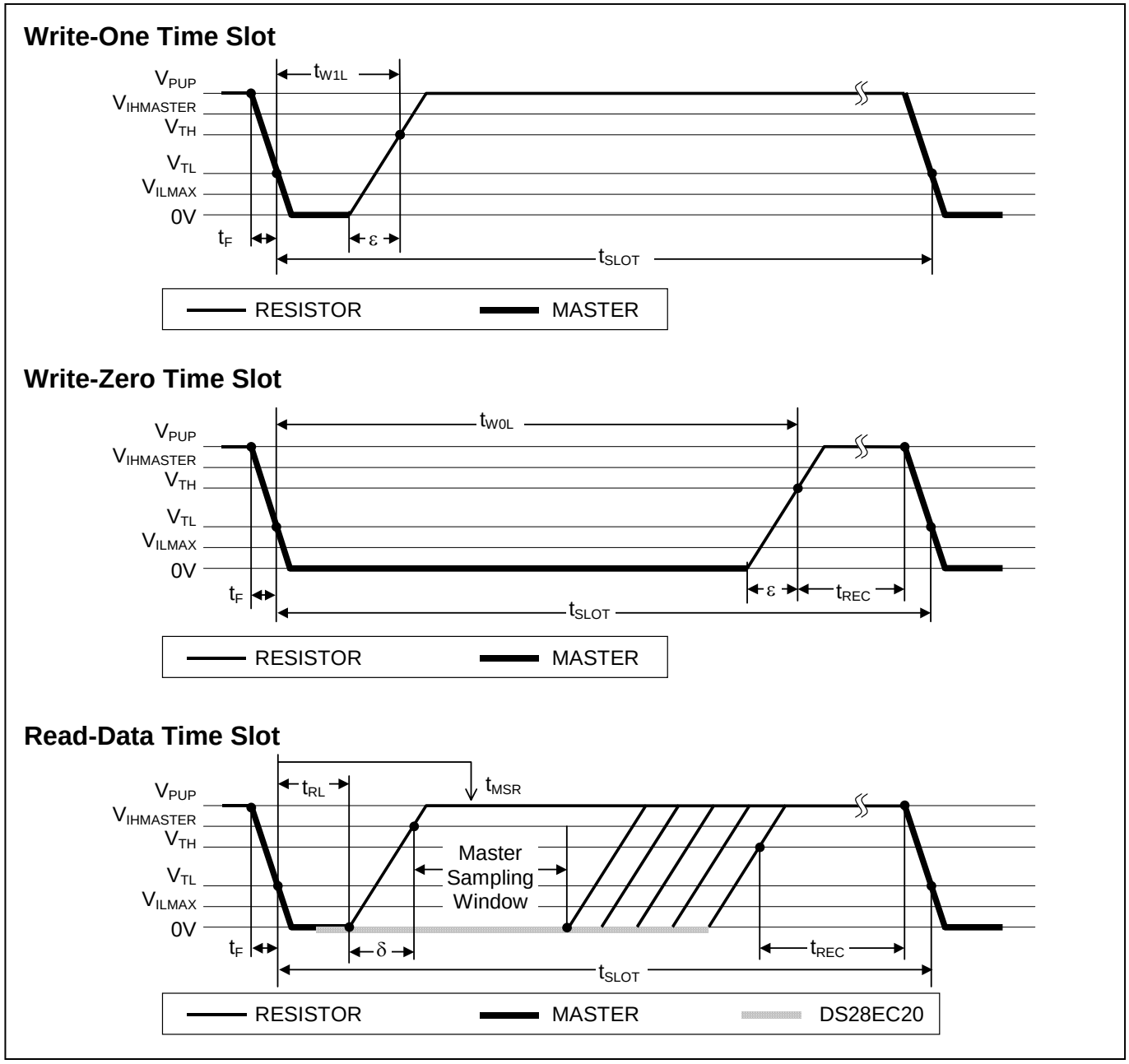
Data communication with the DS28EC20 takes place in time slots, which carry a single bit each. Write-time slots transport data from bus master to slave. Read-time slots transfer data from slave to master. Figure 11 illustrates the definitions of the write- and read-time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28EC20 starts its internal timing generator that determines when the data line is sampled during a write-time slot and how long data is valid during a read-time slot.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28EC20 needs a recovery time t_{REC} before it is ready for the next time slot.

Figure 11. Read/Write Timing Diagram



Slave-to-Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28EC20 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28EC20 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28EC20 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28EC20 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28EC20 attached to a 1-Wire line. For multidevice configurations, t_{REC} needs to be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

IMPROVED NETWORK BEHAVIOR (SWITCHPOINT HYSTERESIS)

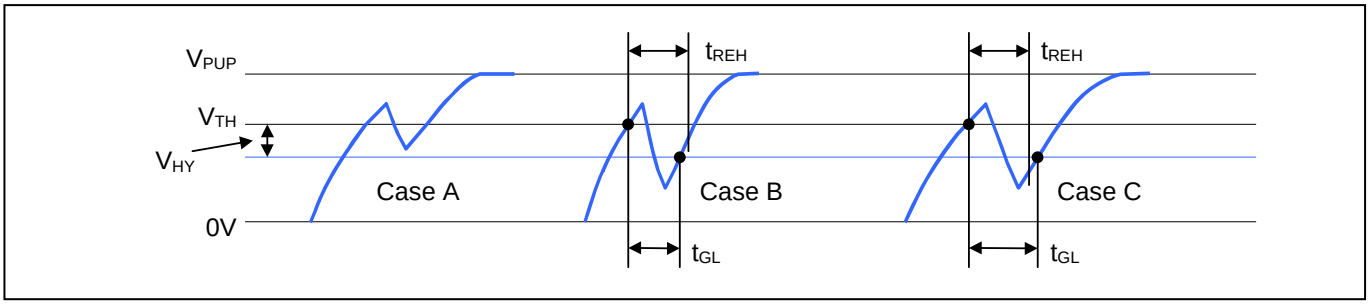
In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28EC20 uses a new 1-Wire front-end, which makes it less sensitive to noise.

The 1-Wire front-end of the DS28EC20 differs from traditional slave devices in three characteristics:

1) There is additional low-pass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
2) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TH} - V_{HY}, it is not recognized (Figure 12, Case A). The hysteresis is effective at any 1-Wire speed.
3) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below V_{TH} - V_{HY} threshold (Figure 12, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 12, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters V_{HY} and t_{REH} specified in their electrical characteristics use the improved 1-Wire front-end.

Figure 12. Noise Suppression Scheme



CRC GENERATION

The DS28EC20 uses two different types of CRCs. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS28EC20 to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form. It is computed at the factory and lasered into the ROM.

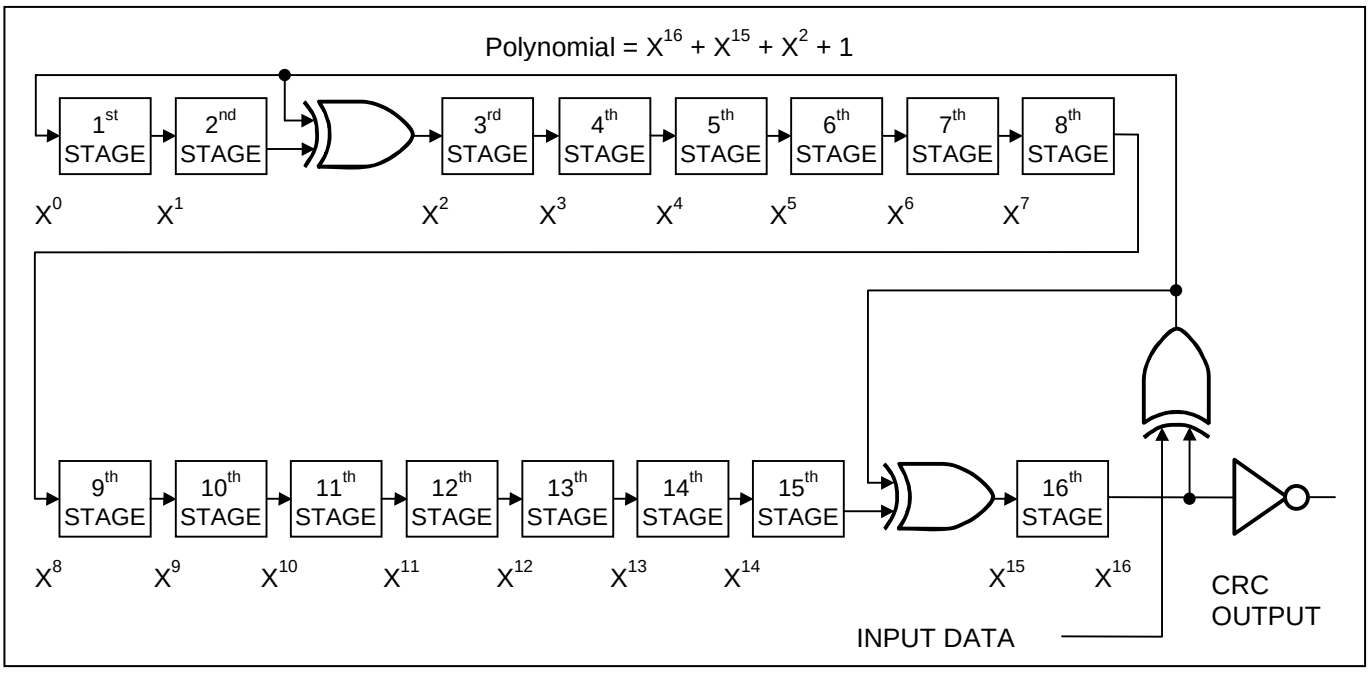
The other CRC is a 16-bit type, generated according to the standardized CRC16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for fast verification of a data transfer when writing to or reading from the scratchpad and with the Extended Read Memory command. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS28EC20 (Figure 13) calculates a new 16-bit CRC, as shown in the command flow chart (Figure 7). The bus master compares the CRC value read from the device to the one it calculates from the data, and decides whether to continue with an operation or to reread the portion of the data with the CRC error.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, and all the data bytes as they were sent by the bus master. The DS28EC20 transmits this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data can start at any location within the scratchpad.

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data as they were sent by the DS28EC20 starting at the target address. The DS28EC20 transmits this CRC only if the reading continues through the end of the scratchpad, regardless of the actual ending offset.

With the initial pass through the extended read memory flow, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the data bytes. Subsequent passes through the extended read memory flow generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes. For more information on generating CRC values refer to *Application Note 27*: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products* (www.maxim-ic.com/AN27).

Figure 13. CRC16 Hardware Description and Polynomial



COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—LEGEND

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master.
PD	1-Wire presence pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol.
WS	Command "Write Scratchpad".
RS	Command "Read Scratchpad".
CPS	Command "Copy Scratchpad".
RM	Command "Read Memory".
ERM	Command "Extended Read Memory".
TA	Target address TA1, TA2.
TA-E/S	Target address TA1, TA2 with E/S byte.
<data to EOS>	Transfer of as many bytes as needed to reach the end of the scratchpad for a given target address.
<data to EOM>	Transfer of as many data bytes as are needed to reach the end of the memory.
<data to EOP>	Transfer of as many data bytes as are needed to reach the end of the page for a given target address.
CRC16\	Transfer of an inverted CRC16.
FF loop	Indefinite loop where the master reads FF bytes.
AA loop	Indefinite loop where the master reads AA bytes.
Programming	Data transfer to EEPROM; no activity on the 1-Wire bus permitted during this time.

COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—COLOR CODES

Master to Slave	Slave to Master	Programming

WRITE SCRATCHPAD (CANNOT FAIL)

RST	PD	Select	WS	TA	<Data to EOS>	CRC16\	FF Loop

READ SCRATCHPAD

RST	PD	Select	RS	TA-E/S	<Data to EOS>	CRC16\	FF Loop

COPY SCRATCHPAD (SUCCESS)

RST	PD	Select	CPS	TA-E/S	Programming	AA Loop

COPY SCRATCHPAD (BS = 1 OR PF = 1 OR COPY PROTECTED)

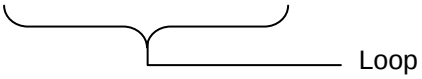
RST	PD	Select	CPS	TA-E/S	FF Loop

READ MEMORY (CANNOT FAIL)

RST	PD	Select	RM	TA	<Data to EOM>	FF Loop

EXTENDED READ MEMORY (CANNOT FAIL)

RST	PD	Select	ERM	TA	<Data to EOP>	CRC16\	<32 Bytes>	CRC16\



PACKAGE INFORMATION

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

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